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DONALD V. TOMKINS
C/O MILLER THOMSON LLP
2700, 10155 - 102 STREET
EDMONTON, AB T5J 4G8
CANADA

EXAMINER	
O BRIEN, BARRY J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 04/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/843,178	GOSIOR ET AL.	
	Examiner	Art Unit	
	Barry J. O'Brien	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 4/26/01, 7/17/01, 3/1/02, 3/14/02,3/3/04.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-18 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-18 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 4.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-18 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Declaration as received on 7/17/2001, Change of Address/POA as received on 3/01/2002, IDS as received on 3/14/2002 and Revocation/Change of Attorney as received on 3/03/2004.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

4. The applicant is requested to review the specification and update the status of all co-pending applications made mention of, replacing attorney docket numbers with current U.S. application or patent numbers when appropriate.

Claim Objections

5. Claims 3 and 8 are objected to because of the following informalities:

a. Claim 3 recites the claim limitation, "'n' multiple groups of independent threads" on its second line. However, "n" is objected to as being indefinite as it is unclear what the bounds on the value "n" can attain. If "n" is a negative number, zero or

a fractional number, the processor will not execute instructions correctly. Similarly, if "n" takes on too great of a number, the number of replicated execution units could become infinite, again causing incorrect function. Please place bounds on the value of the quantity "n" so that it will make the claim language more definite.

b. Claim 8 recites the limitation, "semaphone" on its second line. Please correct the claim language to read, "semaphore".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1, 8, 10-13 and 15-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. Claim 1 recites the limitation "said processor core threads" on its eleventh line. There is insufficient antecedent basis for this limitation in the claim. For the purposes of this examination, the Examiner will assume that this limitation refers to the "independent application threads" defined on the fourth line of the claim.

9. Claim 1 recites the limitation "said instruction set data" on its fourteenth line. There is insufficient antecedent basis for this limitation in the claim. For the purposes of this

examination, the Examiner will assume that this limitation refers to the instructions defined by the instruction set of line nine of the claim.

10. Claim 8 recites the limitation "said peripheral and system memory" on its third and fourth lines. There is insufficient antecedent basis for both the limitation "said peripheral," as well as for "system memory". For the purposes of this examination, the Examiner will assume that the "said peripheral" refers to the peripheral adapter as in claim 1, and that the "system memory" refers to the memory as in claim 1. Furthermore, it is unclear whether the above claim language refers to a peripheral memory and a system memory, or to a peripheral (device) and a system memory. Please correct the claim language to more distinctly claim the invention. The Examiner suggests amending the claim language to read, for example, "said peripheral and said system memory", if that was the case.

11. Claim 10 recites the limitation "said controlling operating processor thread" in the claims first and second lines. There is insufficient antecedent basis for this limitation in the claim. For the purposes of this examination, the Examiner will assume that this limitation refers to a thread that accesses the supervisory control unit. See similar issues in claims 11, 12 and 13 also.

12. Claim 15 recites the limitation "the unassigned bit fields of the machine instructions" on its second and third lines. There is insufficient antecedent basis for this limitation in the claim. Not only is the limitation as a whole not defined in the claims, but also machine instructions are not referred to in the claims alone, nor are bit fields referred to. For the purposes of this examination, the Examiner will assume that these machine instructions reside in one of the application threads executing on the processor as defined in claim 1.

13. Claim 16 recites the limitation, "internal memory for storing and executing core processor code" on its second and third lines. It is unclear how a memory can execute "core processor code", as generally memories only store instructions/code, while an execution unit of some sort executes the instructions. For the purposes of this examination, the Examiner will assume that the internal memory stores core processor code, code that can be executed.

Claim Rejections - 35 USC § 102

14. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

15. Claims 1-3, 6-7, 9-10, 16 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Parady, U.S. Patent No. 5,933,627.

16. Regarding claim 1, Parady has taught a programmable, single chip embedded processor system for input/output applications, comprising:

a. A modular, multiple bit, multithreaded processor core (see Fig.3) operable by at least four parallel and independent application threads sharing common execution logic segmented into a multiple stage processor pipeline (see Fig.3 and Col.3 lines 35-43), wherein said processor core is capable of having at least two states (see Col.3 lines 35-43). Here, the processor supports four threads, each with its own context (or state) using separate register files (see Col.3 lines 44-49).

b. A logic mechanism engaged with said processor core for executing an instruction set within said processor core (41 of Fig.3),

c. A supervisory control unit (112 of Fig.3), controlled by at least one of said processor core threads, for examining said core processor state and for controlling said core processor operation (see Col.3 lines 57-65). Here, the thread switching logic monitors cache misses caused by a thread, and subsequently causes a thread switch. The thread switch is controlled by a current thread which can dictate which thread to switch to (see Col.3 lines 57-65).

d. A memory for storing and executing said instruction set data (see 152 of Fig.5),

e. A peripheral adaptor (178 of Fig.5/6) engaged with said processor core for transmitting input/output signals to and from said processor core (see Figs. 5 and 6).

17. Regarding claim 2, Parady has taught a system as recited in claim 1, wherein said processor pipeline includes an instruction fetch logic stage (see Col.3 lines 2-9), instruction decode logic stage (14 of Fig.3), multiple port register read stage (48/50 of Fig.3), address mode logic stage (see Col.3 lines 2-9), arithmetic logic unit for arithmetic and address calculations stage (see Col.3 lines 50-56), multiple port memory stage (48/50 of Fig.3), branch/wait logic stage (18 of Fig.1), and multiple port register write stage (48/50 of Fig.3). Here, the functions are not shown to be explicit stages of operation in the pipeline, but being that the UltraSparc processor of Parady (see Col.2 lines 66-67) is pipelined (see Col.3 lines 35-43), it is inherent that the operations of these units occur in a pipelined fashion.

18. Regarding claim 3, Parady has taught a system as recited in claim 1, wherein said processor core supports "n" multiple groups of independent threads by replicating said common execution logic and said memory (see Fig.3). Here, n is taken to equal one, and thus Parady has taught one group of four independent threads supported by one replication of the execution logic and memory.

19. Regarding claim 6, Parady has taught a system as recited in claim 1, wherein said instruction set includes a processor instruction for enabling individual threads to determine their thread identity (see Fig.4 and Col.3 line 66 – Col.4 line 8). Here, certain instructions can enable a specific thread upon a thread switch, thus determining the identity of the thread that is desired to be switched to.

20. Regarding claim 7, Parady has taught a system as recited in claim 1, wherein said supervisory control unit (112 of Fig.3) is capable of examining and interpreting the state of multithread processor core operation for the purpose of starting, stopping, and modifying individual multithread processor operation (see Col.3 lines 57-65). Here, the thread switching logic monitors the processing core for a cache miss, and if it determines there was a cache miss, can stop the current thread and start a new thread (see Col.3 lines 57-65), as well as put the threads into interleaving mode (see Col.4 lines 18-29).

21. Regarding claim 9, Parady has taught a system as recited in claim 1, wherein said supervisory control unit is capable of being accessed and controlled by each of said operating core processor threads by using input/output instructions (see Col.3 line 57 – Col.4 line 8). Here, each thread can access the thread switching logic by providing it with a thread ID to switch to

upon a long-latency operation which is detected by the thread switching logic, the thread ID which can be provided in a load or store (input/output) instruction (see Col.4 lines 5-7).

22. Regarding claim 10, Parady has taught a system as recited in claim 9, wherein said controlling operating processor thread is programmable and comprises any of the available threads (see Col.3 line 57 – Col.4 line 8). Here, any of the four threads can cause a cache miss to be detected by the thread switching logic (see Col.3 lines 57-65), and can further be programmed to include a thread field that tells the thread switching logic which thread to switch to (see Col.4 lines 1-8).

23. Regarding claim 16, Parady has taught a system as recited in claim 1, wherein said memory comprises internal memory for storing and executing core processor code (152 of Fig.5) and external memory engaged with said peripheral adaptor (176/180 of Fig.5).

24. Regarding claim 17, Parady has taught a system as recited in claim 1, wherein said supervisory control unit is configured as a peripheral to said processor core (see Fig.3). Here, the thread switching logic is separate from the core functions of fetch, decode, issue and execute.

Claim Rejections - 35 USC § 103

25. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

26. Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parady, U.S. Patent No. 5,933,627 as applied to claim 1 above, and further in view of Dickman et al., U.S. Patent No. 4,556,951.

27. Regarding claim 4, Parady has taught a system as recited in claim 1, but has not explicitly taught wherein the system further comprises a condition code mechanism implemented in said instruction set for detecting specific word data types.

28. However, Dickman has taught a system for detecting specific word data type and setting corresponding condition codes so that conventional program control instructions can be used to control processing, rather than modifying existing control instructions to do so (see Col.2 line 57 – Col.3 line 5). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Parady to detect specific types of data words and set their corresponding condition codes so that existing control instructions can be used, thereby creating less work and preserving the previous compatibility of the instruction set.

29. Regarding claim 5, Parady in view of Dickman has taught a system as recited in claim 4, wherein the value of the least significant byte of a word is detected to be within a specific range (see Col.8 line 63 – Col.9 line 12).

30. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Parady, U.S. Patent No. 5,933,627 as applied to claim 7 above, and further in view of Miyamoto et al., U.S. Patent No. 6,101,569.

31. Regarding claim 8, Parady has taught a system of claim 7, but has not explicitly taught wherein the system further comprises a hardware semaphore vector engaged with said

supervisory control unit for controlling multithread access to said peripheral and system memory.

32. However, Miyamoto has taught a semaphore vector (see Col.5 lines 34-51) which controls multithread access to peripherals and system memory (see Col.4 line 66 – Col.5 line 33) so that data is not inadvertently destroyed by another thread (see Col.1 lines 21-36). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Parady to include the use of hardware semaphore vector to control access to peripherals and memory so that inadvertent data destruction does not take place, and thus incorrect operation does not result.

33. Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parady, U.S. Patent No. 5,933,627 as applied to claim 9 above, and further in view of Fernando et al., U.S. Patent No. 6,272,616.

34. Regarding claim 11, Parady has taught the system as recited in claim 9 above, but has not explicitly taught wherein said controlling operating core processor thread is capable of reconfiguring the overall thread processing method of operation so that other processing threads can support multiple instruction multiple data processing operations.

35. However, Fernando has taught an instruction that allows current processing threads of execution to switch into a SIMD mode or a MIMD mode (see Col.2 lines 58-63) so that processing performance can be increased for a broad range of software types and requirements (see Col.2 lines 27-32). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Parady to allow for an instruction that lets the processing threads switch into MIMD mode in order to improve processing performance for a broad range of software types.

36. Regarding claim 12, Parady has taught the system as recited in claim 9 above, but has not explicitly taught wherein said controlling operating processor thread can reconfigure the overall thread processing method of operation so that other processing threads can support single instruction multiple data processing operations.

37. However, Fernando has taught an instruction that allows current processing threads of execution to switch into a SIMD mode or a MIMD mode (see Col.2 lines 58-63) so that processing performance can be increased for a broad range of software types and requirements (see Col.2 lines 27-32). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Parady to allow for an instruction that lets the processing threads switch into SIMD mode in order to improve processing performance for a broad range of software types.

38. Regarding claim 13, Parady has taught the system as recited in claim 9 above, but has not explicitly taught wherein said controlling operating processor thread is capable of reconfiguring the overall thread processing method of operation so that an arbitrary number of processing threads can support simultaneously single instruction multiple data processing operations and multiple instruction multiple data processing operations.

39. However, However, Fernando has taught an instruction that allows current processing threads of execution to switch into a SIMD mode or a MIMD mode (see Col.2 lines 58-63) so that processing performance can be increased for a broad range of software types and requirements (see Col.2 lines 27-32), which allows SIMD and MIMD modes to be concurrently executing (see Col.12 lines 1-5). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Parady to allow for the processing threads to simultaneously

execute in both SIMD mode and MIMD mode in order to improve processing performance for a broad range of software types.

40. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Parady, U.S. Patent No. 5,933,627 as applied to claim 1 above, and further in view of Bishop et al., U.S. Patent No. 5,784,552.

41. Regarding claim 14, Parady has taught the system as recited in claim 1, but has not explicitly taught wherein said supervisory control unit is operable by a first thread process to start and stop another thread process and to examine and alter state information in single step and multiple step modes of controlled operation.

42. However, Bishop has taught the execution of an application program under the supervision of a debugging program, the debugging program which halts the application program (see Col.5 lines 11-22) and can examine and alter state information via debugging instruction execution in either single-step or multi-step modes of debugging (see Col.7 lines 13-45) so that an application programmer can more thoroughly test and debug their programs in a controlled testing environment (see Col.1 lines 17-35). One of ordinary skill in the art would have recognized that thoroughly tested and debugged programs are less likely to fail and provide incorrect results. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Parady to allow a debugging program to stop and start another program so that instructions in the other program can be thoroughly tested and debugged in both single-step and multi-step modes of debugging.

43. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Parady, U.S. Patent No. 5,933,627 as applied to claim 1 above, and further in view of Zammit et al., European Patent Application No. 1091292.

44. Regarding claim 15, Parady has taught a system as recited in claim 1, but has not explicitly taught wherein the system further comprises identifying bit patterns embedded in the unassigned bit fields of the machine instructions of said core processor.

45. However, Zammit has taught a processor which identifies values in unused bit fields of instruction during a conversion so that the unused bit fields which contain inappropriate values, which could result in incorrect translation, can be corrected before being executed (see p.3 lines 9-16, 35-39). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Parady to identify values of unused bits so that inappropriate values are not incorrectly translated, and thus incorrect execution does not occur. .

46. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Parady, U.S. Patent No. 5,933,627 as applied to claim 1 above, and further in view of Wilske, U.S. Patent No. 4,155,115.

47. Regarding claim 18, Parady has taught a system as recited in claim 1, but has not explicitly taught wherein said peripheral adaptor is capable of controlling analog and digital processing functions.

48. However, Wilske has taught a microprocessor system which has a peripheral controller capable of receiving and controlling inputs from both analog and digital sources (see Col.2 lines 7-34) so that both types of sources can be controlled from one location in order to reduce cost and lessen hardware (see Col.1 lines 14-24). Therefore, one of ordinary skill in the art would

have found it obvious to modify the processor of Parady to allow its peripheral adapter to control both analog and digital sources so that the amount of hardware needed to control both types of sources can be reduced, thus lowering cost.

Conclusion

49. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

50. Joy et al., U.S. Patent No. 6,341,347 has taught a processor which can execute multiple threads simultaneously, and has thread select logic which acts as a supervisor to control the threads.

51. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 6:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

52. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Barry J. O'Brien
Examiner
Art Unit 2183

BJO
4/13/2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100